14. (Twice Amended) A printed circuit board provided with a conductor layer comprising an alignment mark, said alignment mark being electrically isolated from the conductor layer, and in which the conductor layer is comprised of an electroless plated film and an electrolytic plated film.

REMARKS

Reconsideration and withdrawal of the rejections of record are respectfully requested.

Summary of Status of Amendments and Office Action

In the present amendment, claims 1, 2, 7, 13 and 14 are amended, and no claims are canceled. Therefore, claims 1-49 remain pending in the application with claims 1, 2, 6, 7, 9, 11, 13, and 14 being independent.

Claims 6, 8, 11, 12, 46 and 49 are allowed.

Claims 1-5, 7, 9, 10, 13-45, 47 and 48 are rejected.

The specification is objected to under 37 C.F.R. § 1.71 and claims 2, 7, 22-24, 27, 45 and 47 are rejected under 35 U.S.C. § 112, first paragraph.

Claims 1-5, 13-26, 28-45 and 48 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite.

Claims 13-15, 16, 19, 20, 21, 30, 31, 35, 36, 40 and 41 are rejected under 35 U.S.C. § 102(b) as being anticipated by UNO et al., U.S. Patent No. 5,827,604.

Claims 1, 3, 4, 5, 25, 26 and 44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over UNO et al.

Claims 2, 22, 23, 24 and 45 are rejected under 35 U.S.C. § 103(a) as being unpatentable over UNO et al.

Claims 9, 10 and 48 are rejected under 35 U.S.C. § 103(a) as being unpatentable over UNO et al.

Claims 17, 32, 37 and 42 are rejected under 35 U.S.C. § 103 as being unpatentable over UNO et al.

Claims 14, 18, 28, 29, 33, 34, 38, 39 and 43 are rejected under 35 U.S.C. § 103(a) as being unpatentable over UNO et al.

Explanation and Support for Amendments

Applicants submit that each of the foregoing amendments is fully supported by the specification. For the convenience of the Examiner, specific examples of support are noted below:

With regard to the amendment to claims 1 and 2, the claims have been amended to even further clarify that the printed circuit board is a multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits.

With respect to the amendment to claims 13 and 14, and the specification, these have been amended to even more explicitly indicate that the alignment mark is electrically isolated from the conductor layer. This is in accordance with the originally filed application, such as discussed with respect to Figs. 41 and 42 including page 11 et seq. of the specification.

Still further, as will be discussed below, the language of claims 2 and 7 has been clarified with respect to the metal.

Response to Objection Under 37 C.F.R. 1.71 and Rejection of Claims 2, 7, 22-24, 27, 45 and 47 under 35 U.S.C. 112, first paragraph

Applicants note that in this objection and rejection, the Examiner asserts that specification and claims 2, 7, 22-24, 27, 45 and 47 are not enabling because of the language pertaining to the surface of the roughened layer being covered with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal. The rejection contends that copper has an ionization tendency higher than titanium or a noble metal. Therefore, the Examiner suggests that what the Applicant intends is that the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of less than copper but more than titanium or a noble metal.

In contrast to the Examiner's contentions, the present specification and claims are directed to a roughened layer which is covered with a layer of a metal having a ionization tendency of not higher than titanium but more than copper, or the metal is a noble metal. Thus, the metal can be, for example, titanium, aluminum, zinc, iron, indium, thallium, cobalt, nickel, tin, lead, and bismuth, or the metal can be a noble metal such as gold, silver and platinum. In this regard, the Examiner's attention is directed to the originally filed specification, the last two paragraphs on page 18, inter alia.

Applicants note that the amendment herein has even further clarified the claim language, whereby this ground of objection and rejection should be withdrawn.

Response to 35 U.S.C. 112, Second Paragraph, Rejection

Claims 1-5, 13-26, 28-45 and 48 are rejected under 35 U.S.C. 112, second paragraph as being indefinite. In response, Applicants respectfully submit the following.

With respect to claims 1 and 2, the Examiner is basically asserting that these claims are in product by process format and do not set forth positive recitations of structure. In response, Applicants respectfully submit that the claim terminology utilized in claims 1 and 2 is clear and definite, whereby one having ordinary skill in the art would readily comprehend the metes and bounds of the claims. However, in an attempt to advance prosecution of the application, claims 1 and 2 have been amended herein to even more clearly recite that the claims are directed to a multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits.

With regards to claims 3 and 22, the Examiner is asserting that the limitation "the roughened layer is on at least a part of the surface inclusive of a side surface of a conductor circuit" is vague. In response, Applicants respectfully submit that surface can have an upper surface and side surfaces and that the roughened layer can also be on the side surface. Accordingly, the claim language should be considered to be definite.

Thus, Applicants respectfully submit that the claims are clear and definite. However, if the Examiner deems that any amendments to the claims would be beneficial to even further clarify their language, the Examiner is respectfully requested to contact the undersigned by telephone to discuss the same. In this regard, the undersigned has briefly discussed the claimed subject matter with the Examiner during a March 15, 2002 telephone discussion. Moreover, the Examiner indicated that the undersigned can contact him after filing the instant reply to further discuss the application once the Examiner is able to further review the application.

Response to Rejections Base Upon Prior Art

Applicants note that each of the rejections of record relies upon Uno et al., U.S. Patent No. 5,827,604. In this regard, the following rejections are of record:

Claims 13-15, 16, 19, 20, 21, 30, 31, 35, 36, 40 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by UNO.

Claims 1, 3, 4, 5, 25, 26 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over UNO.

Claims 2, 22, 23, 24 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over UNO.

Claims 9, 10 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uno.

Claims 17, 32, 37 and 42 are rejected under 35 § 103 as being unpatentable over UNO.

Claims 14, 18, 28, 29, 33, 34, 38, 39 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over UNO.

In response, Applicants again point out, as in the previous response, that regarding claims 1 and 2, Applicants respectfully submit that UNO fails to disclose or suggest a multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits, said printed circuit board being formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer. In this regard, UNO discloses a structure which has one interlaminar insulating layer 4 on each side of substrate 2. Therefore, UNO fails to disclose or suggest a printed circuit board formed by laminating a first interlaminar insulating layer on a

conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer.

Concerning independent claim 9, Applicants respectfully submit that UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film. In particular, UNO discloses a copper pattern 3, a roughened layer 9 formed by electroless plating, and another film 10 which may be an electrolytic film, (see Examples 6 and 10). In contrast, the viahole of UNO is formed of copper pattern 6. Thus, UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film.

Even if copper pattern 3, roughened layer 9, and layer 10 are somehow considered to be part of the viahole of UNO, then UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film in combination with a roughened layer . . . formed on at least a part of the surface of the underlayer conductor circuit connected to the viahole. As noted above, UNO discloses a copper pattern 3, a roughened layer 9 formed by electroless plating, another film 10 which may be an electrolytic film, and a copper pattern 6. If the copper pattern 3, roughened layer 9, and layer 10 are somehow considered to be part of the viahole, then the viahole would not be connected to a roughened layer. Accordingly, UNO fails to disclose or suggest a viahole comprised of an electroless plated film and an electrolytic plated film in combination with a roughened layer . . . formed on at least a part of the surface of the underlayer conductor circuit connected to the viahole.

For independent claims 13 and 14, Applicants respectfully submit that UNO fails to disclose or suggest an alignment mark, said alignment mark being electrically isolated from the conductor

layer. Applicants note that the Office Action fails to explain where UNO discloses an alignment mark. Accordingly, if for any reason this ground of rejection is maintained in a future Office Action, Applicants request further clarification. Furthermore, since the rejection is not clearly set forth, Applicants respectfully submit that if UNO is relied upon in a future Office Action for this ground of rejection, such an Office Action should be made non-final.

Regarding independent method claims 6, 7, and 11, it is again noted that the Office Action asserts that the method claims are rejected using the same reasoning as applied to the product claims. In response, Applicants respectfully submit that the reasoning supporting this rejection is incomplete and inappropriate, because process claims may be separately patentable and especially considering that the Office Action itself asserts that product-by-process claims are directed to the product per se, no matter how actually made. Since the rejection is not clearly set forth, Applicants respectfully submit that if the Examiner relies upon UNO in a future Office Action for this ground of rejection, such an Office Action should be made non-final.

With respect to each of the rejections set forth above, and as discussed with the Examiner during the above-noted telephone discussion of March 15, 2002, the product limitations in a product by process claim must be given weight. In this regard, the Examiner's attention is directed to MPEP 2113.

However, to expedite prosecution, Applicants respectfully submit that UNO fails to disclose or suggest etching and removing the electroless plated film beneath the plating resist, as recited in independent claims 6, 7, and 11, or forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer, as recited in independent claim

6. In this regard, UNO discloses forming a plating resist 5 which is formed after the interlaminar insulating layer 4. UNO fails to disclose or suggest etching and removing the electroless plated film beneath the plating resist, as recited in independent claims 6, 7, and 11, or forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer, as recited in independent claim 6.

Additionally, each of the dependent claims under this rejection is patentable over the cited documents at least because each of these dependent claims includes the recitations of independent claim 1, 2, 6, 7, 9, 11, 13, or 14. Moreover, each of the dependent claims under this rejection is patentable over the cited documents because it would not have been obvious to a skilled artisan to incorporate such dependent claim features into the invention as more broadly recited in independent claim 1, 2, 6, 7, 9, 11, 13, or 14.

In view of the above, Applicants respectfully request that this ground of rejection be withdrawn.

CONCLUSION

For the reasons advanced above, Applicants respectfully submit that all pending claims patentably define Applicants' invention. Allowance of the application with an early mailing date of the Notices of Allowance and Allowability is therefore respectfully requested.

Should the Examiner have any further comments or questions, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
Motoo ASAI et al.

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APPENDIX
MARKED-UP COPY OF AMENDMENT TO SPECIFICATION

Amendment to the first full paragraph of page 14:

Particularly, the alignment marks 18, 19 are preferably formed in the opening portions exposing only the surface of the conductor layer from the solder resist layer formed on the conductor layer (including the viahole). Because the peripheral edge of the conductor layer overlaps with the solder resist layer and hence the peeling of the conductor can be prevented by holding the conductor with the solder resist layer as shown Fig. 41. Moreover, in the heat cycle, cracks generated starting from the boundary portion between the conductor layer and the interlaminar insulating resin layer due to the difference of thermal expansion coefficient can be controlled. As can be seen, the alignment mark is electrically isolated from the conductor layer.

MARKED-UP COPY OF CLAIM AMENDMENTS

1. (Twice Amended) A multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits, said printed circuit board being formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer on at least a part of the surface of the conductor circuit.

2. (Twice Amended) A multilayer printed circuit board comprising a plurality of interlaminar insulating layers and conductor circuits, said printed circuit board being formed by laminating a first interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer on the first interlaminar insulating layer, wherein the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer on at least a part of the surface of the conductor circuit, and the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but [less] not higher than titanium, or a noble metal.

7. (Twice Amended) A method of producing a multilayer printed circuit board comprising subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit, covering the surface of the roughened layer with a layer of

a metal having an ionization tendency of more than copper but [less] not higher than titanium, or a noble metal, and forming an interlaminar insulating layer.

13. (Twice Amended) A printed circuit board provided with a conductor layer comprising an alignment mark, said alignment mark being electrically isolated from the conductor layer, and in which a roughened layer is formed on at least a part of the surface of the conductor layer.

14. (Twice Amended) A printed circuit board provided with a conductor layer comprising an alignment mark, said alignment mark being electrically isolated from the conductor layer, and in which the conductor layer is comprised of an electroless plated film and an electrolytic plated film.